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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FRANCISCUS PETRUS WIDDERSHOVEN

Appeal 2008-3064
Application 10/023,165
Technology Center 2100

Decided: December 4, 2008

Before JAMES D. THOMAS, LEE E. BARRETT, and JOSEPH L. DIXON, *Administrative Patent Judges*.

DIXON, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

A Patent Examiner rejected claims 1-4. The Appellant appeals therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

A. INVENTION

The invention at issue on appeal relates to "a data processing device with a memory. Some types of memory suffer from wear. Data stored in memories that suffer from wear can only be changed a limited number of times before the stored data becomes unreliable. In current flash memory for example, the data can only be changed some 100000 times before there is significant wear." (Spec. 1). Appellant further describes the invention as follows:

> To promote the availability of codewords, the WOM code is such that a second data value can be coded after a first data value and vice versa without changing back bits. That is, the code contains a first and second codeword that represent the first data value and a third and fourth codeword that represent the second data value. The third codeword can be written over the first codeword without changing back bits and the second codeword can be written over the fourth codeword without changing back bits. The bits that have been changed initially to write the first or fourth codeword for the first and second data value respectively also differentiate the subsequent third and second codeword from other codewords, ensuring efficient use of code bits.
>
> . . . .
>
> Preferably, the data processing circuit has a plurality of such series of locations, each corresponding to a different logical address. When a processor addresses a series with a logical address, data is written or read in the currently active one of the locations of the series that is addressed by the logical address. Preferably, the memory comprises a matrix of rows and columns, where each row can be addressed and reset as a whole, the series of locations comprising an integer number of at least one of such rows.

(Spec. 2).

B. ILLUSTRATIVE CLAIM

Claim 1, which further illustrates the invention, follows:

1. A data processing device comprising a memory having locations, each capable of storing a WOM codeword from a WOM code; a memory selector for selecting a currently selected location of a logical series of the locations; a data encoder that encodes a received data value in a new codeword from the WOM code, as a function of the received data value and a previous codeword stored in the currently selected location, the data encoder causing the currently selected location to be changed to a next one in the logical series when the WOM code is exhausted, the data encoder storing the new codeword in the currently selected location; a reset circuit for resetting a content of the locations in the logical series, the reset circuit being triggered when the WOM code is exhausted for all the locations of the logical series.

C. REFERENCES

The Examiner relies on the following references as evidence:

Rivest	US 4,691,299	Sep. 1, 1987
Sinclair	US 6,069,827	May 30, 2000
Estakhri	US 6,772,274 B1	Aug 3, 2004

D. REJECTIONS

The Examiner makes the following rejections:

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivest, Sinclair, and Estakhri.

II. ISSUE

Has the Examiner set forth a sufficient prima facie showing of obviousness of the claimed invention?

III. PRINCIPLES OF LAW

35 U.S.C. § 103(a)

> Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1734 (2007).

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," and discussed circumstances in which a patent might be determined to be obvious. *KSR,* 127 S. Ct. at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966)). The Court reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at 1740.

The Federal Circuit recently recognized that "[a]n obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case. Indeed, the common sense of those skilled in the art demonstrates why some combinations would have been

obvious where others would not." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (citing *KSR*, 127 S. Ct. 1727, 1739 (2007)). The Federal Circuit relied in part on the fact that Leapfrog had presented no evidence that the inclusion of a reader in the combined device was "uniquely challenging or difficult for one of ordinary skill in the art" or "represented an unobvious step over the prior art." *Id.* at 1162 (citing *KSR*, 127 S. Ct. at 1740-41).

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

IV. ANALYSIS

With respect to independent claim 1, we agree with the Examiner that the teachings of Rivest are quite relevant to the instant claimed invention which utilizes WOM (write-once memory) code since its teachings are discussed at page 1 of Appellant's Specification relative to individual WOM codes. We find the teachings of Sinclair and Estakhri clearly less relevant to the instant claimed invention utilizing a WOM code in a memory comprising selectable locations of a series of locations and encoding using the logical series of memory locations when the WOM code is exhausted and then a reset circuit for resetting the content of the location ends in the logical series being triggered when the WOM code is exhausted for all of the locations of the logical series as recited in independent claim 1

Here, the teachings of Rivest are with respect to a memory location that stores a singular codeword and not to a series of logical locations as recited in independent claim 1.

The Examiner relies upon the teaching of Estakhri which identifies a current sector associated with a range of logical block addresses (Answer 4), but the Examiner does not rationalize how the use of a current sector in a flash memory would provide motivation to a skilled artisan to expand the teachings of Rivest using a block of three bits for a WOM code to use a logical series of memory locations greater than the three bit WOM code.

Additionally, the Examiner relies upon the teachings of Sinclair with regards to the erasable write-once type memory which is arranged in blocks which the Examiner analogizes to a logical series of memory locations in which a storage location must be erased when it is exhausted/used (Answer 5), but the Examiner does not state a rationale of how the use of a write-once memory would provide motivation to a skilled artisan to expand the teachings of Rivest using a block of three bits for a WOM code to use a logical series of memory locations greater than the three bit WOM code to reset the logical series of locations when all locations have been exhausted as set forth in the last element of independent claim 1.

Here, we find the Examiner has attempted to reconstruct using hindsight reconstruction the elements of independent claim 1. Furthermore, even if the elements were combined, we find that the combination would not have taught or fairly suggested the invention as recited in independent claim 1. Essentially, the claimed invention is an expansion of the three bit WOM code to sequential iterations using and keeping track of a sequence of memory locations to thereby extend the life of the memory beyond the limited scope of the three bit WOM code. The Examiner has not identified any teachings of Sinclair, Estakhri, or Rivest which suggest the modification

as recited in the claimed invention. Therefore, we will reverse the rejection of independent claim 1 and its respective dependent claims 2-4.

V. CONCLUSION

For the aforementioned reasons, the Examiner has not set forth a sufficient prima facie showing of obviousness of the claimed invention.

VI. ORDER

We reverse the obviousness rejections of claims 1-4.

REVERSED

msc

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